CLAIMS

We claim:

1. A programmable logic device comprising:

volatile memory adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory adapted to store data which is transferable to the volatile memory to configure the programmable logic device;

a first data port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory; and

a second data port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

2. The programmable logic device of Claim 1, further comprising control logic adapted to transfer the data from the non-volatile memory to the volatile memory to configure the programmable logic device.

3. The programmable logic device of Claim 1, further comprising core logic adapted to be configured by the configuration data stored in the volatile memory.

4. The programmable logic device of Claim 1, wherein the volatile memory comprises static random access memory and the non-volatile memory comprises flash memory.

5. The programmable logic device of Claim 1, wherein the non-volatile memory is further adapted to store security bits that can be set to prevent unauthorized reading of the data from the programmable logic device.

6. The programmable logic device of Claim 1, wherein the first data port is a JTAG port and the second data port is a CPU port.

7. The programmable logic device of Claim 6, wherein the first data port supports an IEEE 1149.1 standard, with the external data transferred to the non-volatile memory and/or the volatile memory via an IEEE 1532 programming mode or to the non-volatile memory via a background programming mode.

8. The programmable logic device of Claim 6, wherein the external data is transferred through the second data port to the volatile memory via a system configuration mode, to the non-volatile memory directly, and/or to the non-volatile memory via a background programming mode.

9. The programmable logic device of Claim 1, wherein the programmable logic device further supports reading back of the configuration data stored in the volatile memory and/or the data stored in the non-volatile memory for verification.

10. The programmable logic device of Claim 9, wherein the programmable logic device further supports the reading back while the programmable logic device performs its intended function based on the configuration data stored by the volatile memory.

11. The programmable logic device of Claim 1, wherein the programmable logic device supports transfer of the external data to the non-volatile memory while the programmable logic device is operable to perform its intended logic functions.

12. A programmable device comprising:

static random access memory adapted to configure the programmable device for its intended function based on configuration data stored by the static random access memory;

flash memory adapted to store data which is transferable to the static random access memory to configure the programmable device;

a JTAG port adapted to receive external data for transfer into either the static random access memory or the flash memory;

a CPU port adapted to receive external data for transfer into either the static random access memory or the flash memory; and

means for transferring the external data received by the JTAG port or the CPU port to the static random access memory or the flash memory.

13. The programmable device of Claim 12, wherein the means comprises:

a background mode adapted to transfer the external data from the JTAG port to the flash memory or transfer the external data from the CPU port to the flash memory;

a programming mode adapted to transfer the external data from the JTAG port to the flash memory and/or to the static random access memory; and

a system configuration mode adapted to transfer the external data from the CPU port to the static random access memory.

14. The programmable device of Claim 13, wherein the background mode and the programming mode are further adapted to support readback of data stored in the flash memory and the static random access memory.

15. The programmable device of Claim 13, wherein the JTAG port supports an IEEE 1149.1 standard and the programming mode supports an IEEE 1532 standard.

16. The programmable device of Claim 12, further comprising control logic adapted to transfer the data from the flash memory to the static random access memory to configure the programmable device.

17. The programmable device of Claim 12, further comprising core logic adapted to be configured by the data stored in the static random access memory.

18. A method of providing programming options for a programmable device, the method comprising:

providing a background mode for transferring external data via a first data port or a second data port to non-volatile memory;

providing a direct mode for transferring the external data via the second data port to the non-volatile memory; and

providing a system configuration mode for transferring the external data via the second data port to volatile memory, wherein the volatile memory is adapted to configure the programmable device.

19. The method of Claim 18, wherein the background mode is further adapted to readback the external data stored in the non-volatile memory and the volatile memory.

20. The method of Claim 18, wherein the first data port is adapted to support a JTAG standard and the second data port is adapted to provide a CPU interface.

21. The method of Claim 18, further comprising providing a programming mode for transferring the external data via the first data port to the non-volatile memory or to the volatile memory.

22. The method of Claim 21, wherein the programming mode is further adapted to readback the external data stored in the non-volatile memory and the volatile memory

23. The method of Claim 21, wherein the programming mode is further adapted to support an IEEE 1532 standard.

24. The method of Claim 18, further comprising providing a transfer mode for transferring the external data stored in the non-volatile memory to the volatile memory.

25. A programmable logic device comprising:

volatile memory adapted to configure the programmable logic device for its intended function based on configuration data stored by the volatile memory;

non-volatile memory adapted to store data which is transferable to the volatile memory to configure the programmable logic device; and

a CPU port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

26. The programmable logic device of Claim 25, wherein the volatile memory comprises static random access memory and the non-volatile memory comprises flash memory.

27. The programmable logic device of Claim 25, wherein the programmable logic device supports transfer of the external data through the CPU port to the non-volatile memory while the programmable logic device is operable to perform its intended logic functions.

28. The programmable logic device of Claim 25, further comprising a JTAG port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory.

29. The programmable logic device of Claim 28, wherein the data stored in the volatile memory is transferable directly to the non-volatile memory.

30. The programmable logic device of Claim 28, wherein the data stored in either the volatile memory or the non-volatile memory is transferable out of the programmable logic device via the CPU port or the JTAG port and transferable into the non-volatile memory or the volatile memory via the JTAG port or the CPU port, respectively, to complete a cross port transfer of the data.

31. A method of providing data transfer options for a programmable logic device, the method comprising:

providing a CPU port adapted to receive external data for transfer into either volatile memory or non-volatile memory of the programmable logic device, wherein data stored in the volatile memory configures the programmable logic device; and

providing data registers adapted to transfer data stored in the non-volatile memory to the volatile memory and to transfer data stored in the volatile memory to the non-volatile memory.

32. The method of Claim 31, wherein the volatile memory comprises static random access memory and the non-volatile memory comprises flash memory.

33. The method of Claim 31, further comprising providing a JTAG port adapted to receive the external data for transfer into either the volatile memory or the non-volatile memory of the programmable logic device.

34. The method of Claim 33, wherein the CPU port and the JTAG port provide cross port data transfer capability between the volatile memory and the non-volatile memory.

35. The method of Claim 31, wherein the programmable logic device supports transfer of the external data through the CPU port to the non-volatile memory while the programmable logic device is operable to perform its intended logic functions.